

combination thereof. The step of forming opening 48B is optional as the final shape of the replacement channel opening could be non-V shape (opening 48A only) or V-shape (opening 48A in addition to 48B).

After the opening 48A and the optional opening 48B are formed, the replacement channel 50 may be formed in the opening 48A as illustrated in FIGS. 14A through 14C. The replacement channel region 50 may induce a strain and/or allow higher mobility in the channel region so that the FinFET device 200 may have better device performance. The replacement channel region 50 may be formed by epitaxially growing SiGe, Si, SiP, Ge, the like, or a combination thereof in the 48A with an optional cap layer of Si over the replacement channel region 50. The growth of the replacement channel region 50 may be substantially confined by the dielectric layer 22 and the semiconductor strip 24. As illustrated in FIGS. 14A and 14C, sidewalls of the replacement channel region 50 may be substantially orthogonal to the top surface of the semiconductor substrate 20 and a top surface of the replacement channel region 50 may substantially parallel with the top surface of the semiconductor substrate 20. In an embodiment, the top surface of the replacement channel region 50 may be substantially coplanar with a top surface of the dielectric layer 22 and the top surface of the semiconductor strip 24. In another embodiment, the top surface of the replacement channel region 50 may be below or above the top surface of the dielectric layer 22 and the semiconductor strip 24.

In a PMOS embodiment, the replacement channel region 50 may comprise SiGe_x (where $x \geq 0.1$) and may be doped with boron. In an NMOS embodiment, the replacement channel region 50 may comprise Si and may be doped with phosphorous. In both the NMOS and PMOS embodiments, the replacement channel 50 may include a Si cap layer over the replacement channel region 50.

After the replacement channel region 50 is formed, the fins 29 may be formed by an etch process to recess the dielectric layer 22 in the area under the opening 42 as illustrated in FIGS. 15A through 15C. This fin formation step may be performed by similar processes as described in the fin formation of FIGS. 5A and 5B, and is not repeated herein. In an embodiment, the dielectric layer 22 may be recessed beneath the opening 42 (see FIG. 15C), but not in the areas surrounding the source region 30 and the drain region 28 (see FIG. 15B).

FIGS. 16A through 16C illustrate the formation of gate dielectric layer 44 and gate 46 in the opening 42 and over the replacement channel region 50. The gate dielectric layer 44 and gate 46 may be formed of similar materials and by similar processes as gate dielectric layer 26 and gate 32 described in FIGS. 2A and 2B, and are not repeated herein. As shown in FIG. 16C, the gate 46 and the gate dielectric layer 44 adjoins three sides of the fin 29.

By forming the fins 29 after the source regions 30 and the drain regions 28 have been formed, the shape of source regions 30 and the drain regions 28 may be controlled and confined by the dielectric layer 22. This control and confinement will reduce or eliminate the faceting of the source regions 30 and the drain regions 28 which will reduce the resistance of the subsequent metal layers contacting the source regions 30 and the drain regions 28. Also, the facets on the source regions 30 and the drain regions 28 may allow the subsequent metal layers to leak through the intersection of the facets. Further, by replacing the channel region with a replacement channel region 50, the FinFET device 200 may have better performance due to the strain inducing and/or high mobility channel region.

FIGS. 17 through 31 illustrate in cross-sectional views along a semiconductor strip 24 (A-A line of FIG. 1) of various stages in the manufacture of a PMOS FinFET 400 and an NMOS FinFET 300, both in a Fin-Last, Gate-Last, Replacement Channel configuration according to another embodiment. Details regarding this embodiment that are similar to those for the previously described embodiments will not be repeated herein.

FIG. 17 illustrates an NMOS FinFET 300 and a PMOS FinFET 400 with each of the NMOS and PMOS FinFETs 300 and 400 comprising a source region 30 and a drain region 28. The source regions 30 and the drain region 28 are formed in a semiconductor strip 24 with and ILD 40 formed over the semiconductor strip 24 and the dummy gates 38.

FIG. 18 illustrates an ESL 60 formed over the ILD 40 and the dummy gates 38 and a hard mask layer 62 formed over the ESL 60. The ESL 60 may be formed of an oxide, a nitride, the like, or a combination thereof and the hard mask layer 62 may be formed of SiN, SiON, SiO₂, the like, or a combination thereof.

In FIG. 19, a bottom anti-reflective coating (BARC) layer 64 is formed over the hard mask layer 62. The BARC layer 64 prevents radiation in a subsequent photolithographic process to reflect off layers below and interfering with the exposure process. Such interference can increase the critical dimension of the photolithography process. The BARC layer 64 may be formed by CVD, the like, or a combination thereof. A photoresist 66 may be deposited and patterned over the BARC layer 64. After developing and removing a portion of the photoresist 66, an etch step is further performed into the BARC layer 64 to expose the portion of the hard mask layer 62 over the NMOS FinFET 300. FIG. 20 illustrates the transferring of the photoresist 66 pattern to the hard mask layer 62 to expose the NMOS FinFET 300.

In FIG. 21, the dummy gate 38 of the NMOS FinFET 300 is removed and a channel region below the dummy gate 38 is removed. A first etch may be performed to form opening 68 and a second etch may be performed to form opening 70 in the semiconductor strip 24. This step may be performed in a similar manner as described above in reference to FIGS. 12A through 12C and will not be repeated herein. FIG. 22 illustrates the formation of a V-shape opening 72 below the opening 70. This step may be performed in a similar manner as described above in reference to FIGS. 13A through 13C and will not be repeated herein.

FIG. 23 illustrates the formation of a V-shaped NMOS replacement channel region 74 in the openings 70 and 72. This step may be performed in a similar manner as described above in reference to FIGS. 14A through 14C and will not be repeated herein. FIG. 24 illustrates the removal of the hard mask layer 62 and the ESL 60 over the PMOS FinFET device 400. This step may be performed by an etch comprising H₃PO₄, a DHF treatment, the like, or a combination thereof.

FIG. 25 illustrates the formation of another ESL 76 and a hard mask layer 78 over the ILD 40 and the NMOS and PMOS FinFETs 300 and 400. The ESL 76 and the hard mask layer 78 may be deposited in the opening 68, wherein the ESL 76 adjoins the gate spacers 34 and at top surface of the V-shaped NMOS replacement channel region 74. This step may be performed in a similar manner as described above in reference to FIG. 18 and will not be repeated herein. FIG. 26 illustrates the formation of another BARC layer 80 and a photoresist 82 that is patterned to expose the hard mask layer 78 over the PMOS FinFET 400. This step may be performed in a similar manner as described above in reference to FIG. 19 and will not be repeated herein. FIG. 27 illustrates the